

QUESTION 2015

Group – A (Multiple Choice Type Questions)

1. Choose the correct alternatives for the following:
- i) The compiler optimization technique is used to reduce
- a) cache miss penalty
 - ✓ b) cache miss rate
 - c) cache hit time
 - d) none of these
- ii) The CPI value for RISC processors is
- ✓ a) 1
 - b) 2
 - c) 3
 - d) more
- iii) The vector stride value is required
- ✓ a) to deal with the length of vectors
 - b) to find the parallelism in vectors
 - c) to access the elements in multi-dimensional vectors
 - d) none of these
- iv) The task of a vectorizing compiler is
- a) to find the length of vectors
 - b) to convert sequential scalar instructions into vector instructions
 - c) to process multi-dimensional vectors
 - ✓ d) to execute vector instructions
- v) Utilization pattern of successive stages of a synchronous pipeline can be specified by
- a) truth table
 - b) excitation table
 - ✓ c) reservation table
 - d) periodic table
- vi) The UMA multiprocessor system is best suited
- a) when the degree of interaction among different modules in program is large
 - b) when the degree of interaction among different modules in program is less
 - c) when there is no interaction among different modules in program
 - ✓ d) when different programs are to be executed concurrently
- vii) The cache coherence is a potential problem especially
- a) in asynchronous parallel algorithm execution in multiprocessor
 - b) in synchronous parallel algorithm execution in multiprocessor
 - ✓ c) in asynchronous parallel algorithm execution in data flow m/c
 - d) in synchronous parallel algorithm execution in data flow m/c
- viii) A direct mapped cache memory with n blocks is nothing but which of the following set associative cache memory organization?
- ✓ a) 0-way set associative
 - b) 1-way set associative

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| Instruction type | Instruction count | Clock cycle count |
|---------------------------|-------------------|-------------------|
| Integer arithmetic | 50000 | 1 |
| Data transfer | 35000 | 2 |
| Floating point arithmetic | 20000 | 2 |
| Branch | 6000 | 3 |

Calculate the effective CPI, MIPS rate and execution time for this program.

c) Why do we need parallel processing? What are different levels of parallel processing? Explain.

a) See Topic: RISC & CISC ARCHITECTURES, Long Answer Type Question No. 1 (a).

b) See Topic: RISC & CISC ARCHITECTURES, Long Answer Type Question No. 1 (b).

c) See Topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Long Answer Type Question No. 4.

8. a) What is meant by pipeline hazard? Briefly discuss different pipeline hazards.

b) What do you mean by job collision in pipeline processor? Show how collisions occur in the following static pipeline.

| | 0 | 1 | 2 | 3 | 4 |
|-------|---|---|---|---|---|
| S_0 | X | | | | X |
| S_1 | | X | | X | |
| S_2 | | | X | | |

c) Consider the execution of a program of 20,000 instructions by a linear pipeline processor with a clock rate 40 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-order executions are ignored. Calculate the speed-up of the pipeline over its equivalent non-pipeline processor, the efficiency and throughput.

a) See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 13 (a).

b) See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 13 (b).

c) See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 13 (c).

9. a) Why do we need masking mechanism in SIMD array processors?

In an SIMD array processor of 8 PEs, the sum $S(k)$ of the first k components in a vector A is desired for each k from 0 to 7. Let $A = (A_0, A_1, \dots, A_7)$. We need to compute the following and

throughput. $S(k) = \sum_{i=0}^k A_i$; for $k = 0, 1, \dots, 7$

Discuss how data-routing and masking are performed in the processor.

b) How do vector processors improve the speed of instruction execution over scalar processors? Illustrate with an example.

c) What is vectorizing compiler? Why do we need it in a vector processor?

a) See Topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Short Answer Type Question No. 2.

b) See Topic: VECTOR PROCESSOR, Long Answer Type Question No. 3 (a).

c) See Topic: VECTOR PROCESSOR, Long Answer Type Question No. 3 (b).

10. a) What is the basic objective of data flow architecture? Compare it with control flow architecture.

b) What is meant by the cache miss penalty? Briefly discuss "early restart" technique to reduce miss penalty.

c) Let us consider a memory system consisting of main memory and cache memory. In case of a cache miss, assume the performance of the basic memory organization as:

- 4 clock cycles to send the address
- 24 clock cycles for the access time per word
- 4 clock cycles to send a word of data.

i) What will be the miss penalty, given a cache block of four words?

ii) What will be the memory bandwidth?

a) See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 1.

b) See Topic: MEMORY, Long Answer Type Question No. 7 (a).

c) See Topic: MEMORY, Long Answer Type Question No. 7(b).

11. a) Compare and contrast RISC and CISC computers. Give one example for each.

b) What is multi-processor system? Classify it with examples.

c) Design $2^2 \times 3^2$ Delta network.

a) See Topic: RISC & CISC ARCHITECTURES, Short Answer Type Question No. 1.

b) See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 8.

c) See Topic: INTERPROCESS COMMUNICATION, Short Answer Type Question No. 10.

QUESTION 2016

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following:

i) The main memory of a computer has $2m$ blocks while the cache has $2c$ blocks. If the cache uses the set associative mapping scheme with 2 blocks per set; then block k of the main memory maps to the set

a) $(k \bmod m)$ of the cache

✓ b) $(k \bmod c)$ of the cache

c) $(k \bmod 2m)$ of the cache

d) $(k \bmod 2c)$ of the cache

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ii) Suppose the time delay of the four stages of a pipeline are $t_1 = 60$ ns, $t_2 = 50$ ns, $t_3 = 90$ ns, $t_4 = 80$ ns respectively and the interface latch has a delay $t_l = 10$ ns, then the maximum clock frequency for the pipeline is

- a) 100 ns ✓ b) 90 ns c) 190 ns d) 30 ns

iii) As the bus in a multiprocessor is a shared resource, so there must be some mechanism to resolve the conflict. The algorithm from the below mentioned is not a conflict resolution technique.

- ✓ a) state priority algorithm b) FIFO algorithm
c) LRU algorithm d) Daisy Chaining algorithm

iv) Dynamic pipeline allows

- ✓ a) multiple functions to evaluate b) only streamline connection
c) perform fixed function d) none of the above

v) A computer with cache access time of 100 ns, a main memory access time of 1000 ns and a hit ratio of 0.9 produces an average access time of

- a) 250 ns b) 200 ns ✓ c) 190 ns d) 80 ns

vi) The number of cycles required to complete n tasks in a k stage pipeline is

- ✓ a) $k + n - 1$ b) $nk + 1$ c) k d) none of these

vii) The prefetching technique is a solution for

- a) data hazard b) structural hazard
✓ c) control hazard d) enhancing the speed of pipeline

viii) In general an n input Omega network requires stages of 2×2 switches.

- a) 2 b) 4 c) 8 d) 16

Answer: NONE OF THESE. Answer is $\log_2 n$.

ix) Which of the following has no practical usage?

- a) SISD b) SIMD ✓ c) MISD d) MIMD

x) The expression for Amdahl's law is

- ✓ a) $S(n) = 1/f$ where $n \rightarrow \infty$ b) $S(n) = f$ where $n \rightarrow \infty$
c) $S(n) = 1/T$ where $n \rightarrow \infty$ d) none of these

Group – B

(Short Answer Type Questions)

2. If there are no stalls (waits) then prove that the speedup is equal to the pipeline depth i.e., the number of pipeline stages.

OR,

Show that the maximum speedup of a pipeline is equal to its stages.

See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 1.

3. Draw pipeline execution diagram during the execution of the following instructions:

MUL R1, R2, R3

ADD R2, R3, R4

INC R4

SUB R6, R3, R7

Find out the delay in pipeline execution due to data dependency of the above instructions.

See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 18.

4. How "Reservation Table" helps to study the performance of pipeline.

See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 19.

5. What do you mean cache coherence problem? Describe one method to remove this problem and its limitations.

See Topic: MEMORY, Short Answer Type Question No. 10.

6. Consider the execution of a program of 15000 instructions by linear pipeline processor. The clock rate of pipeline is 25 MHz. Pipeline has five stages and one instruction is issued per clock cycle. Neglect pipelines due to branch instructions and out of sequence execution:

(i) Calculate the speedup program execution by pipeline as compared with that by non-pipelined processor.

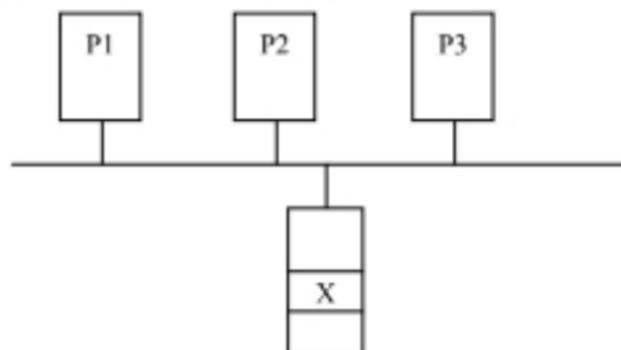
(ii) What are the efficiency and throughput of the pipeline processor.

See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 20.

Group – C

(Long Answer Type Questions)

7. What is the difference between broadcast and invalidate protocols? Explain MESI protocol. What is the difference between centralized shared memory and distributed shared memory? Explain superscalar, super-pipelined and VLIW processors.



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The value of X (shared memory) is 50. P1 and P3 want to read X and store in their cache memories. At t1 time P1 wants to write on X for three times. After that P3 wants to read for two times. After that first P3 writes on X and then P2 wants to read.

Explain the above mentioned scenario using Write through update, Write back update, Write through invalidate. Write back invalidate protocols.

1st part: See Topic: MEMORY, Long Answer Type Question No. 8.

2nd part: See Topic: MEMORY, Long Answer Type Question No. 8.

3rd part: See Topic: INTERPROCESS COMMUNICATION, Short Answer Type Question No. 11.

4th part: See Topic: VECTOR PROCESSING, Short Answer Type Question No. 4.

5th part: See Topic: MEMORY, Long Answer Type Question No. 8.

8. Explain Flynn's classification. What are the differences between loosely coupled system and tightly coupled system? Construct a multiport network where three processing elements want to connect with three memory modules. Design a network where 9 inputs want to connect with 25 outputs. What is the difference between omega network and delta network? Construct an omega network for $N = 8$ where N represent no. of processors.

1st part: See Topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Short Answer Type Question No. 1.

2nd part: See Topic: INTERPROCESS COMMUNICATION, Short Answer Type Question No. 6.

Rest part: See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 9.

9. a) Consider the following pipeline reservation table.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|----|---|---|---|---|---|---|---|---|
| S1 | X | | | | | X | | X |
| S2 | | X | | X | | | | |
| S3 | | | X | | X | | X | |

b) What are the forbidden latencies?

c) Draw the state transition diagram.

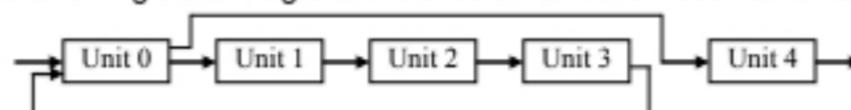
d) List all the simple cycles and greedy cycles.

e) Determine the optimal constant latency cycle and the minimal average latency.

f) Let the pipeline clock period be $\tau = 20ns$. Determine the throughput of the pipeline.

See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 14.

10. a) Consider the following block diagram of a circuit. Form the Reservation table.



b) An instruction requires four stages to execute:

Stage 1 (instruction fetch) requires 30 ns:

Stage 2 (instruction decode) = 9 ns, stage 3 (instruction execute) = 20 ns and stage 4 (store results) = 10 ns. An instruction must proceed through the stages in sequence. What is the minimum asynchronous time for any single instruction to complete?

c) We want to set this up as a pipelined operation. How many stages should we have and at what rate should we clock the pipeline?

See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 16.

11. a) With the use of Amdahl's law, conclude, among the given options which possible improvement is the best one.

| Instruction type | Frequency | CPI |
|------------------|-----------|-----|
| ALU | 40% | 1 |
| Branch | 20% | 4 |
| Load | 30% | 2 |
| Store | 10% | 3 |

Possible improvements:

1. Branch CPI can be decreased from 4 to 3.
2. Increase clock frequency from 2 to 2.3 GHz.
3. Store CPI can be decreased from 3 to 2.

b) What do you mean by memory fragmentation? What is the advantage of using Paging? Explain Virtual memory concept with an example where logical address space is 8 kb, physical address space is 4 kb, page size is 1 kb. Explain page fault with FIFO and LRU Algorithm.

a) See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 15.

b) See Topic: MEMORY, Long Answer Type Question No. 9.

QUESTION 2017

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following:

i) CPI of super scalar pipeline is

- ✓ a) less than 1 b) more than 1 c) 1 d) none of these

ii) Pipelining uses

- ✓ a) data parallelism b) temporal parallelism
c) spatial parallelism d) none of these

iii) Utilization pattern of successive stages of a synchronous pipeline are specified by

- a) Truth table b) Excitation time
✓ c) Reservation table d) Periodic table

iv) Dynamic pipeline allows

- ✓ a) multiple functions to evaluate b) only streamline connection

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- c) perform fixed function
d) none of these
- v) the equations for Amdahl's law is
a) $S(n) = 1/f$ where $n \rightarrow \infty$
✓c) $S(n) = 1/T$ where $n \rightarrow \infty$
b) $S(n) = f$ where $n \rightarrow \infty$
d) none of these
- vi) Array Processors are put under which one of the following categories?
a) SISD ✓b) SIMD c) MISD d) MIMD
- vii) The number of cycles required to complete n tasks in a k stage pipeline is
✓a) $k+n-1$ b) $nk-1$ c) k d) none of these
- viii) An n -dimensional hypercube has
a) n^n nodes b) n^{-n} nodes ✓c) 2^n nodes d) none of these
- ix) Which of the following is a recursive network?
a) Benes network b) Baseline network
c) Cross bar network ✓d) none of these
- x) The compiler optimization technique is used to reduce
a) cache miss penalty ✓b) cache miss rate
c) cache hit time d) none of these

Group – B

(Short Answer Type Questions)

2. "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement.

See topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 13.

3. a) Write down Amdahl's law of parallel processing.

b) Suppose, you have a program that has 10% code portion which must be executed sequentially. Now further suppose that we are to employ parallel programming to achieve a speedup. How many parallel processors must be there to achieve an overall speedup of 5 in the program execution time?

a) See topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 21.

b) *Incomplete data*

4. What is branch hazard? Briefly discuss two methods to handle branch hazards.

See topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 6(d).

5. What do you mean by cache coherence problem? Describe one method to remove this problem and its limitations.

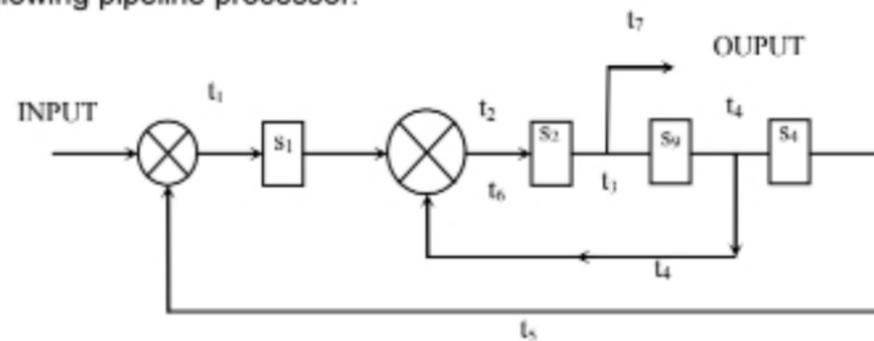
See topic: MEMORY, Short Answer Type Question No. 10.

6. What is the drawback of direct mapped cache? How is it resolved in set associative cache?

See topic: MEMORY, Short Answer Type Question No. 17.

Group – C
(Long Answer Type Questions)

7. Consider the following pipeline processor:



Where, S = number of stages & T = clock cycles

S_i is number of stages and T_i is clock cycle

- Specify the reservation table for this pipeline with six columns and four rows.
- List the set of forbidden latencies between task initiations.
- Draw the state diagram which shows all possible latency cycles.
- List all greedy cycles from the state diagram.
- What is the value of minimal average latency?
- What is the maximal throughput of this pipeline?

See topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 17.

8. a) A computer has 512kB cache memory and 2MB main memory. If the block size is 64 bytes then find subfield for

- associative memory
- direct mapping
- set-associative mapping

b) How does cache memory increase the speed of processing? Explain.

See topic: MEMORY, Long Answer Type Question No. 10.

9. a) Explain different types of addressing modes?

- What are the advantages of Relative addressing mode over Direct addressing mode?
- Differentiate between Vectored and Non-vectored interrupts.

a) & b) See topic: RISC & CISC ARCHITECTURES, Long Answer Type Question No. 2.

c) See topic: VECTOR PROCESSOR, Long Answer Type Question No. 4.

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10. a) With the help of a neat diagram show the structure of a typical arithmetic pipeline performing $(A*B+C)$

b) A hierarchical cache main memory sub-system has the following specifications:

Cache access time: 50 ns

Main memory access time: 500 ns

80% of memory request for read

Hit ratio: 0.9 for read access and write through scheme is used.

i) Calculate the average access time of the memory system considering only memory read cycle

ii) Calculate the average access time of memory system both read and write cycle.

a) See topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 18.

b) See topic: MEMORY, Long Answer Type Question No. 11.

11. a) Discuss about Flynn's classification of parallel computers.

b) What is the significance of interconnection network in multiprocessor architecture?

c) What are the differences between loosely coupled and tightly coupled architectures?

a) See topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Short Answer Type Question No. 1.

b) See topic: INTERPROCESS COMMUNICATION, Short Answer Type Question No. 7.

c) See topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 4(c).

QUESTION 2018

Group – A

(Multiple Choice Type Questions)

1. Answer any *ten* of the following questions. Choose the correct answer from the given options:

i) A Pipeline stage

a) is a sequential circuit

b) is a combinational circuit

✓c) consists of both sequential and combinational circuit

d) None of the above

ii) Utilization pattern of successive stages of a synchronous pipeline can be specified by

a) Truth table

b) Excitation table

✓c) Reservation table

d) Periodic table

iii) Compiler optimization technique is used to reduce

a) cache miss penalty

✓b) cache miss rate

c) cache hit time

d) None of these

iv) The MMX technology uses

a) Pipelining technique

b) Vectorizing technique

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Group – B (Short Answer Type Questions)

2. Explain the main factors that can influence the performance of the interconnection networks.
See Topic: **INTERPROCESS COMMUNICATION, Long Answer Type Question No. 5.**
3. What is vector chaining? How can it speedup the processing? Explain with suitable example.
See Topic: **VECTOR PROCESSOR, Short Answer Type Question No. 10.**
4. Explain in brief with neat diagrams the Flynn's classifications of computers.
See Topic: **FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Short Answer Type Question No. 1.**
5. What do you mean by hazards in pipeline? Describe the different types of hazards.
See Topic: **PIPELINE ARCHITECTURE, Short Answer Type Question No. 7.**
6. Explain the C-access and S-access memory organizations for vector accesses.
See Topic: **INTERPROCESS COMMUNICATION, Short Answer Type Question No. 12.**

Group – C (Long Answer Type Questions)

7. a) Consider the four-stage pipelined processor specified by the following reservation table:

| | 1 | 2 | 3 | 4 |
|----|---|---|---|---|
| S1 | X | | X | |
| S2 | | X | | |
| S3 | | | X | |
| S4 | | X | | X |

- (i) List the set of forbidden latencies and collision vector.
 - (ii) Draw the state transition diagram.
 - (iii) List all simple cycles from state diagram.
 - (iv) Identify the simple cycles among greedy cycles.
 - (v) Find out minimum average latency
- See Topic: **PIPELINE ARCHITECTURE, Long Answer Type Question No. 11(b).**

- b) Describe different types of vector instructions.
See Topic: **VECTOR PROCESSOR, Short Answer Type Question No. 2.**

8. a) What are the differences between loosely coupled system and tightly coupled system?
- b) What do you mean by multiple issue processor?
- c) Write the differences between scalar processor and vector processor.
- d) Discuss the techniques to achieve instruction level parallelism.

- e) Explain low-order interleaved memory and its advantages.
- a) See Topic: INTERPROCESS COMMUNICATION, Short Answer Type Question No. 6.a).
- b) See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 8(a).
- c) See Topic: VECTOR PROCESSOR, Long Answer Type Question No. 6(a).
- d) See Topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Short Answer Type Question No. 4.
- e) See Topic: VECTOR PROCESSOR, Long Answer Type Question No. 5.

9. a) What are the differences between the static network and the dynamic network?
b) What do you mean by bisection width and diameter of a network?
c) Differentiate between vector processor and array processor with example.
d) What are the differences between shared memory multiprocessor system and message passing multi-computer system?
e) Explain software parallelism and hardware parallelism.
- a), b) & c) See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 10.
 - e) See Topic: VECTOR PROCESSOR, Long Answer Type Question No. 2(b).
 - d) See Topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Long Answer Type Question No. 3.

10. a) Explain the concept of locality of reference and state its importance to memory systems.
b) What is cache mapping? What is set associative mapping in cache memory?
c) What is cache memory? How does it increase the performance of a computer? What is miss penalty?
d) What are the three different types of cache misses? Explain the technique to reduce the cache miss.
- a) See Topic: MEMORY, Short Answer Type Questions No. 11.
 - b) See Topic: MEMORY, Long Answer Type Question No. 12.
 - c) See Topic: MEMORY, Long Answer Type Question No. 3.
 - d) See Topic: MEMORY, Short Answer Type Question No. 8.

11. Write the short notes any three of the following:

- a) Compare CISC and RISC
 - b) Cache coherence problem and its solution
 - c) The VLIW processor architecture
 - d) Cluster computer
 - e) Data flow computer
- a) See Topic: RISC & CISC ARCHITECTURES, Short Answer Type Question No. 1.
 - b) See Topic: MEMORY Long Answer Type Question No. 13.b).
 - c) See Topic: PIPELINE ARCHITECTURE Long Answer Type Question No. 21(e).
 - d) See Topic: RISC & CISC ARCHITECTURES, Long Answer Type Question No. 3(c).
 - e) See Topic: PIPELINE ARCHITECTURE Long Answer Type Question No. 21(f).

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QUESTION 2019

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following:

i) What will be the speed up for a 4 segment linear pipeline when the number of instruction $n = 64$?

- a) 4.5 ✓b) 3.82 c) 8.16 d) 2.95

ii) Virtual address can be divided into some fixed size fields of

- a) segments b) blocks ✓c) pages d) tags

iii) Which is not the property of a memory module?

- a) inclusion ✓b) capability
c) locality d) consistency

iv) In absence of TLB, to access a physical memory location in a page – memory system, how many memory accesses are required?

- a) 4 b) 3 ✓c) 2 d) 1

v) A pipeline stage

- a) is sequential circuit b) is combinational circuit
✓c) both (a) and (b) d) none of these

vi) Which of the following is not the possible cause of data hazard?

- a) RAW ✓b) RAR c) WAW d) WAR

vii) In which of the following shared memory multiprocessor models the time to access shared memory is same?

- a) NORMA b) COMA ✓c) UMA d) NUMA

viii) Utilization pattern of successive stages of a synchronous pipeline can be specified by

- ✓a) reservation table b) truth table
c) excitation table d) periodic table

ix) In which type of processor array processing is possible?

- ✓a) SIMD b) MIMD c) MISD d) SISD

x) In which type of memory mapping conflict miss occurs?

- a) set associative ✓b) direct
c) associative d) only (a) & (b)

- xi) The fastest data access is provided using
a) caches b) DRAM's c) SRAM's ✓ d) registers
- xii) The throughput of a super scalar processor is
a) less than 1 b) 1
✓ c) more than 1 d) not known

Group – B
(Short Answer Type Questions)

2. Differentiate between 3-address, 2-address, 1-address and 0-address instructions with suitable example.

See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 22.

3. What is instruction cycle? Compare and contrast hardwired vs. micro programmed control unit.

See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 23.

4. What is Von-Neumann architecture? What is a Von-Neumann bottleneck? How can this be reduced?

See Topic: RISC & CISC ARCHITECTURES, Short Answer Type Question No. 3.

5. Describe Flynn's classification of computer?

See Topic: FLYNN'S TAXONOMY OF COMPUTER ARCHITECTURE, Short Answer Type Question No. 1.

6. Compare RISC and CISC architecture in brief.

See Topic: RISC & CISC ARCHITECTURES, Short Answer Type Question No. 1.

Group – C
(Long Answer Type Questions)

7. a) Differentiate between multiprocessors and multi computers based on their structures, resource sharing and inter processor communication.

b) With the help of neat sketches, explain the 10 subsystems in case of lightly coupled multiprocessor system.

a) See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 4.a)

b) See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 11.

8. a) What is cache memory? Define global miss & local miss with a suitable example.

b) Describe different technique to reduce cache Miss Penalty.

c) Describe different techniques to reduce cache miss rate.

a) See Topic: MEMORY, Long Answer Type Questions No. 3.a)

b) See Topic: MEMORY, Long Answer Type Question No. 3.b)

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c) See Topic: MEMORY, Short Answer Type Question No. 8.

9. Consider the following pipeline reservation table

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|----|---|---|---|---|---|---|---|---|
| S1 | X | | | | | X | | X |
| S2 | | X | | X | | | | |
| S3 | | | X | | X | | X | |

- Find forbidden and permissible latency set
- Draw the state transition diagram
- Find all simple cycles
- Find the minimum average latency
- What are the performance measuring parameters of a pipelining system? Explain briefly.

See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 19.

10. a) Simplify the following program segment using internal forwarding and register tagging techniques:

$R0 \leftarrow (M1)$

$R0 \rightarrow (R0)+(M2)$

$R0 \rightarrow (R0)*(M2)$

$M4 \rightarrow (R0)$

b) How data hazards are detected and prevented?

a) See Topic: PIPELINE ARCHITECTURE, Long Answer Type Question No. 20.

b) See Topic: PIPELINE ARCHITECTURE, Short Answer Type Question No. 7.

11. Write short notes on any *three* of the following:

- Virtual memory
- Multiprocessor computer
- RISC
- TLB
- Paging.

a) See Topic: MEMORY, Long Answer Type Question No. 13.c).

b) See Topic: INTERPROCESS COMMUNICATION, Long Answer Type Question No. 12.f).

c) See Topic: RISC & CISC ARCHITECTURES, Long Answer Type Question No. 3.d).

d) See Topic: MEMORY, Long Answer Type Question No. 13.d).

e) See Topic: MEMORY, Long Answer Type Question No. 13.e).

